**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (Currently amended) A driving method of speaker for converting digital sound data into corresponding driving signals to drive said speaker, the driving method comprising the steps of:

dividing said digital sound data into at least two data groups, including a first data group and a second data group;

modulating said first data group into a first driving signal, wherein the magnitude of said first data group is represented by pulse width of said first driving signal;

converting ~~a first input signal based on~~ said second data group into a second driving signal according to said second data group and under the control of a second input signal based on said first driving signal, wherein the magnitude of said second data group is represented by pulse height of said second driving signal;

outputting a speaker driving signal according to at least said first driving signal and said second driving signal; and

driving said speaker according to said speaker driving signal.

2. (Previously presented) The driving method as set forth in claim 1, wherein said first data group is higher bits data group and said second data group is lower bits data group.

3. (Previously presented) The driving method as set forth in claim 1, wherein said first data group is lower bits data group and said second data group is higher bits data group.

4. (Currently amended) A driving circuit of speaker for converting digital sound data into corresponding driving signals to drive said speaker, said digital sound data being divided into at least two data groups including a first data group and a second data group, the driving circuit comprising:

a pulse width modulation circuit being used to modulate said first data group into a first driving signal, wherein the magnitude of said first data group is represented by pulse width of said first driving signal; and

a pulse height conversion circuit being used to convert ~~said a first input signal based on~~ said second data group into a second driving signal according to said second data group and under the control of a second input signal based on said first driving signal, and to output a speaker driving signal according to at least said first driving signal and said second driving signal, wherein the magnitude of said second data group is represented by pulse height of said second driving signal;

wherein said speaker is driven according to said speaker driving signal.

5. (Previously presented) The driving circuit of speaker as set forth in claim 4, wherein the pulse width modulation circuit comprises:

a counter;

an accumulator having one input terminal connected to said first data group;

a first comparator for comparing the output of said counter with the output of said accumulator;

a second comparator for comparing the output of the counter with the first data group; and

a XOR gate having two input terminals being connected to the outputs of said first comparator and the second comparator, respectively.

6. (Previously presented) The driving circuit of speaker as set forth in claim 5, wherein the counter starts counting from 0 at the beginning of every sound sampling cycle.

7. (Previously presented) The driving circuit of speaker as set forth in claim 5, wherein the output of the first comparator is HI when the counting value of said counter is smaller than the output value of said accumulator.

8. (Previously presented) The driving circuit of speaker as set forth in claim 7, wherein the output of the second comparator is HI when the counting value of said counter is smaller than the output value of said first data group.

9. (Previously presented) The driving circuit of speaker as set forth in claim 5, wherein the pulse height conversion circuit comprises:

a plurality of AND gates, one input terminal of each of said AND gates being commonly connected to the output of said XOR gate, and the other input terminal of each of said AND gates being respectively connected to the second data group; and

a plurality of current sources with different current ratios, controlled by the output of said AND gates and the output of the second comparator, the output of said current sources being commonly connected to said speaker.

10-16. (Canceled)

17. (Previously presented) A driving circuit of speaker for converting digital sound data into corresponding driving signals to drive said speaker, said digital sound data being divided into a higher bits data group and a lower bits data group, the driving circuit comprising:

a pulse width modulation circuit being used to modulate said higher bits data group into driving signals represented by pulse width, the pulse width modulation circuit comprising:

a counter;

an accumulator having one input terminal connected to said higher bits data group;

a first comparator for comparing the output of said counter with the output of said accumulator;

a second comparator for comparing the output of the counter with the higher bits data group; and

an XOR gate having two input terminals being connected to the outputs of said first comparator and the second comparator, respectively; and

a pulse height conversion circuit being used to convert said lower bits data group into driving signals represented by pulse height.

18. (Previously presented) The driving circuit of speaker as set forth in claim 17, wherein the counter starts counting from 0 at the beginning of every sound sampling cycle.

19. (Previously presented) The driving circuit of speaker as set forth in claim 17, wherein the output of the first comparator is HI when the counting value of said counter is smaller than the output value of said accumulator.

20. (Previously presented) The driving circuit of speaker as set forth in claim 19, wherein the output of the second comparator is HI when the counting value of said counter is smaller than the output value of said higher bit data group.

21. (Previously presented) The driving circuit of speaker as set forth in claim 17, wherein the pulse height conversion circuit comprises:

a plurality of AND gates, one input terminal of each of said AND gates being commonly connected to the output of said XOR gate, and the other input terminal of each of said AND gates being respectively connected to the lower bits data group; and

a plurality of current sources with different current ratios, controlled by the output of said AND gates and the output of the second

comparator, the output of said current sources being commonly connected to said speaker.

22. (Withdrawn) The driving method as set forth in claim 1, wherein said step of converting said second data group comprises:

receiving a logic output signal obtained by said first driving signal and a comparator output signal, wherein said comparator output signal is obtained by comparing an added data group based on said first data group with a counting value which is used to determine the pulse width of said first driving signal; and

converting said first input signal into said second driving signal according to said second data group and under the control of said second input signal, wherein said first input signal corresponds to said second data group and said second input signal corresponds to said logic output signal.

23. (Withdrawn) The driving method as set forth in claim 22, wherein said step of outputting a speaker driving signal comprises:

obtaining an output signal whose pulse height corresponds to the pulse weight of said first driving signal; and

outputting said speaker driving signal according to said second driving signal and said output signal.

24. (Withdrawn) The driving method as set forth in claim 23, wherein said first data group is higher bits data group and said second data group is lower bits data group.

25. (Withdrawn) The driving method as set forth in claim 1, wherein said step of converting said second data group comprises:

obtaining an added data group based on said second data group;

selecting one of said added data group and said second data group as said first input signal under the control of said second input signal, wherein said second input signal corresponds to said first driving signal; and

converting said first input signal into said second driving signal according to said second data group.

26. (Withdrawn) The driving method as set forth in claim 25, wherein said step of outputting a speaker driving signal comprises:

outputting said second driving signal as said speaker driving signal.

27. (Withdrawn) The driving method as set forth in claim 26, wherein said first data group is lower bits data group and said second data group is higher bits data group.

28. (Currently amended) The driving circuit of speaker as set forth in claim 4, wherein the pulse height modulation circuit comprises:

an accumulator for obtaining an added data group based on said second data group;

a multiplexer for selecting one of said added data group and said second data group as [[said]] a first input signal under the control of said second input signal, wherein said second input signal corresponds to said first driving signal; and

a plurality of current sources with different current ratios, controlled by

said first input signal, for converting said first input signal into said second driving signal according to said second data group, wherein said second driving signal is based on output of said current sources, wherein said speaker driving signal corresponds to said second driving signal.

29-30. (Canceled)

31. (New) A driving circuit for generating a plurality of driving signals according to a plurality of digital signals, each of the digital signals including a plurality of bits and representing one value, the driving circuit generating a first driving signal of the plurality of driving signals according to a first digital signal of the plurality of digital signals, the driving circuit comprising:

a pulse height modulation circuit for generating a first part of the first driving signal according to the first digital signal;

a pulse width modulation circuit for generating a second part of the first driving signal according to the first digital signal; and

a node coupled to the pulse height modulation circuit and the pulse width modulation circuit for outputting the first driving signal according to the first and second parts of the first driving signal;

wherein a waveform of the first part of the first driving signal is different from a waveform of the second part of the first driving signal in at least one of pulse height and pulse width such that a waveform of the first driving signal is discontinuous.

32. (New) The driving circuit of claim 31, wherein the pulse height modulation circuit generates the first part of the first driving signal according to a first part of a plurality of bits of the first digital signal such that the pulse height of the first part of the first driving signal varies with the first part of the plurality of bits of the first digital signal.

33. (New) The driving circuit of claim 32, wherein the pulse width modulation circuit generates the second part of the first driving signal according to a second part of the plurality of bits of the first digital signal such that the pulse width of the second part of the first driving signal varies with the second part of the plurality of bits of the first digital signal.

34. (New) The driving circuit of claim 33, wherein the waveform of the first driving signal has a number of levels in pulse width which is determined by the second part of the plurality of bits of the first digital signal.

35. (New) The driving circuit of claim 32, wherein the waveform of the first driving signal has a number of levels in pulse height which is determined by the first part of the plurality of bits of the first digital signal.

36. (New) The driving circuit of claim 31, wherein the plurality of digital signals are digital sound data.